
SURFACE
AND THIN FILMS

Epitaxial Low-Temperature Growth of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ Films on GaAs(100) and GaAs(111)A Substrates Using a Metamorphic Buffer

G. B. Galiev^a, I. N. Trunkin^c, E. A. Klimov^a, A. N. Klochkov^a, A. L. Vasiliev^{b,c}, R. M. Imamov^b,
S. S. Pushkarev^{a,*}, and P. P. Maltsev^a

^a Institute of Ultra High Frequency Semiconductor Electronics, Russian Academy of Sciences, Moscow, 117105 Russia

^b Shubnikov Institute of Crystallography, Federal Scientific Research Centre “Crystallography and Photonics,”
Russian Academy of Sciences, Moscow, 119333 Russia

^c National Research Centre “Kurchatov Institute,” Moscow, 123182 Russia

*e-mail: serp456207@gmail.com

Received March 16, 2016

Abstract—A complex investigation of epitaxial $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ films grown on GaAs substrates with crystallographic orientations of (100) and (111)A in the standard high- and low-temperature modes has been performed. The parameters of the GaAs substrate and $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ film were matched using the technology of step-graded metamorphic buffer. The electrical and structural characteristics of the grown samples have been studied by the van der Pauw method, atomic force microscopy, scanning electron microscopy, and transmission/scanning electron microscopy. The surface morphology is found to correlate with the sample growth temperature and doping with silicon. It is revealed that doping of low-temperature $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers with silicon significantly reduces both the surface roughness and highly improves the structural quality. Pores 50–100 nm in size are found in the low-temperature samples.

DOI: 10.1134/S1063774517060104

INTRODUCTION

The importance of growing epitaxial films of $\text{A}^{\text{III}}\text{B}^{\text{V}}$ compounds by molecular-beam epitaxy (MBE) in the low-temperature mode [1–4] is related to the possibility of using them as materials for photoconductive antennas: THz generators and detectors [3–5]. One of these materials is low-temperature GaAs (LT-GaAs), which is characterized by an ultrashort lifetime of photoexcited carriers, high resistivity, and high electron mobility [2]. The peculiar properties of LT-GaAs are due to the presence of excess As atoms in the volume of grown epitaxial film, which lead to the formation of point defects: substitutional defects (substitution of As atoms for Ga atoms, As_{Ga}), interstitial As atoms (As_i), and vacancies at Ga atomic sites (V_{Ga}). The As_{Ga} concentration exceeds that of V_{Ga} by a factor of about 10^3 . Specifically As_{Ga} defects are suggested to be responsible for the capture of photoexcited carriers and decrease in their lifetime [6].

Photoconductive antennas based on LT-GaAs operate under irradiation at a wavelength of $\sim 0.8 \mu\text{m}$, a value corresponding to the GaAs band gap ($\sim 1.4 \text{ eV}$). This fact limits the range of choice of lasers that can operate with this antenna. A Ti:sapphire laser with a

wavelength of $0.8 \mu\text{m}$ is generally used for photoexcitation of LT-GaAs-based antennas [7].

To shift the photoconductive-antenna pump wavelength to the practically important wavelength regions of 1.3 and $1.56 \mu\text{m}$, where available and inexpensive fiber lasers can be applied, one should develop a material with a band gap of $\sim 0.8 \text{ eV}$. This requirement is satisfied by $\text{In}_x\text{Ga}_{1-x}\text{As}$ solid solutions with an indium molar fraction $x \sim 0.5$, which have intensely been investigated recently [8–10].

$\text{In}_x\text{Ga}_{1-x}\text{As}$ layers can be grown on InP substrates; however, these substrates are small, expensive, and brittle. For this reason, the formation of $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers on GaAs substrates using the metamorphic buffer (MB) technology appears more promising.

The MB formation technology has been studied in detail and is actively applied when preparing InAlAs/InGaAs/InAlAs nanoheterostructures on GaAs substrates for field transistors and low-noise amplifiers of millimeter wave band [11–14]. In contrast to $\text{In}_x\text{Al}_{1-x}\text{As}$ metamorphic layers, $\text{In}_x\text{Ga}_{1-x}\text{As}$ metamorphic layers are mainly used in heterostructures for optoelectronic devices [15–18] grown at conventional temperatures (400°C or higher). At the same time, to the best of our knowledge, there are no data in

Active layer $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$		660 nm
Metamorphic buffer	$\text{In}_{0.55}\text{Ga}_{0.45}\text{As}$	60 nm
	$\text{In}_{0.50}\text{Ga}_{0.50}\text{As}$	60 nm
	$\text{In}_{0.45}\text{Ga}_{0.55}\text{As}$	60 nm
	$\text{In}_{0.40}\text{Ga}_{0.60}\text{As}$	60 nm
	$\text{In}_{0.35}\text{Ga}_{0.65}\text{As}$	60 nm
	$\text{In}_{0.30}\text{Ga}_{0.70}\text{As}$	60 nm
	$\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$	60 nm
	$\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$	60 nm
	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	60 nm
	$\text{In}_{0.10}\text{Ga}_{0.90}\text{As}$	60 nm
	$\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$	60 nm
GaAs		35 nm
GaAs (100) or (111) <i>A</i> substrate		—

Fig. 1. Design of the samples.

the literature on application of GaAs substrates using the metamorphic technology for preparation of LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ low-temperature layers.

The purpose of this study was to analyze the microstructural (including surface morphology) and electrical characteristics of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ epitaxial films grown on GaAs(100) and GaAs(111)*A* substrates in the high- and low-temperature modes. The designation (111)*A* implies that Ga atoms are present on the (111) surface. The GaAs(100) and GaAs(111)*A* substrates were used to determine the influence of the substrate surface orientation on the microstructure and electrical properties of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ or LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ epitaxial layers in the presence of MB.

EXPERIMENTAL

An $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ epitaxial layer was formed on a GaAs substrate using the technology of preliminary MB formation with respect to the thick $\text{In}_x\text{Ga}_{1-x}\text{As}$ transition layer with a chemical composition varying over depth, which is located between the substrate and active layer (in our case, $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layer). This layer successively reduces the lattice mismatch between the GaAs substrate and $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layer. The MB design may be different [19–21]. In this study, we chose the MB design that allows for a stepwise change in the indium molar fraction x (as in [21]).

The samples were prepared by MBE on semi-insulating GaAs(100) and GaAs(111)*A* substrates. To

reach the maximum identity of the technological conditions (growth temperature and ratio of the V- and III-group element flows, $\gamma = P_{\text{As4}}/P_{\text{Ga+In}}$) in one process, two halves of the GaAs substrates of different orientations were mounted onto the sample holder. The samples grown on the GaAs(100) and GaAs(111)*A* substrates will be denoted as (sample no.)-0 and (sample no.)-1, respectively. The sample design is shown in Fig. 1. A buffer GaAs layer 35 nm thick was grown directly on the initial substrates at a standard growth temperature of 510°C. In regards to the MB growth conditions, the samples can be divided into two groups: samples with the MB grown at a standard high temperature (2V and 3V) and samples with the MB grown at a lower temperature (4V and 5V). The temperature modes of MB formation for different samples are presented in Fig. 2. The $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layers in the samples of series 2V and 3V were grown at a temperature of 450°C, whereas in the samples of series 4V and 5V they were grown at 200°C (i.e., they are LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers in this case). In addition, the active layers in samples 2V and 4V were undoped, whereas in samples 3V and 5V they were homogeneously doped with Si atoms. The doping of the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layers was performed at a silicon-cell temperature of 1120°C. In the case of high-temperature growth of *n*-GaAs on the GaAs(100) substrate, this value corresponds to a volume electron concentration of $(3-4) \times 10^{18} \text{ cm}^{-3}$. The choice of the flow ratio γ of V- and III-group elements is related to the choice of the conductivity type: it is known that the doping of high-temperature GaAs epitaxial layers on GaAs(111)*A* substrates with silicon induces *p*-type conductivity at $\gamma = 16-36$ [22, 23]. In this study, these growth conditions were applied to the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers to obtain *p*-type conductivity (Table 1). Note that the chosen technological growth conditions may be non-optimum for the simultaneous formation of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers on GaAs(100) and GaAs(111)*A* substrates. Nevertheless, the chosen approach of simultaneous growth of samples on two substrates in the same processing cycle makes it possible to compare the microstructure specific features and electrical characteristics of the samples grown on different substrates.

The electrical characteristics (mobility and two-dimensional concentration of charge carriers) were determined by the van der Pauw method at room temperature. The sample surfaces were analyzed by atomic force microscopy (AFM) using a Solver Next microscope and scanning electron microscopy (SEM). The crystal structure was studied by transmission/scanning electron microscopy (TEM/STEM) using transverse cuts prepared according to the standard technique [24]. The samples were investigated in a TITAN 80-300 TEM/STEM transmission scanning electron microscope (FEI, United States) equipped with a spherical aberration corrector for a condenser

system, high-angle dark-field detector (Fischione, United States), and energy-dispersive X-ray spectrometer (EDAX, United States) at an accelerating voltage of 300 kV. The images were analyzed using the Digital Micrograph (Gatan, United States) and TIA (FEI, United States) software.

RESULTS AND DISCUSSION

Electrical Characteristics

Note that all samples were grown at the γ values for which a layer of standard high-temperature GaAs doped with Si atoms acquires p -type conductivity in the case of growth on a GaAs(111) A substrate and n -type conductivity for the growth on a GaAs(100) substrate [22, 23]. However, $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers of all the samples under study have n -type conductivity. This fact suggests that the GaAs(111) A surface properties, which determine the amphoteric properties of Si atoms on this surface, are not transferred through the MB.

The values of electron mobility and concentration at a temperature of 300 K are listed in Table 2. According to these data, samples 2V-0 and 2V-1 have high electron concentrations (corresponding to the values for undoped high-temperature $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers), which is due to the narrow band gap of this material. The electron mobility in sample 2V-0 is high, which indicates a high structural quality of the MB.

These results indicate also that the doping of all samples increases significantly the electron concentration and slightly increases the electron mobility. This effect may be related to the screening of charged defects by electrons and, accordingly, weaker electron scattering from defects.

All the samples on GaAs(111) A substrates are characterized by a lower electron mobility as compared with similar samples on GaAs(100) substrates (by a factor of 2.5–8.3). This fact can be explained by the poor structural quality of the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ films grown on GaAs(111) A substrates.

A comparison of pairs of samples 2V and 4V shows that the electron concentration in the low-temperature LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers is higher than that in the standard high-temperature layers of the same composition by about an order of magnitude, whereas the electron mobility is lower. This can be explained by the formation of a large number of antisite defects As_{Ga} during the low-temperature growth, which are, on the one hand, electron donors and, on the other hand, charged scattering centers.

Surface Morphology

The surface morphology of epitaxial structures is known to depend on many factors. The governing factor is the choice of the optimal growth mode, which,

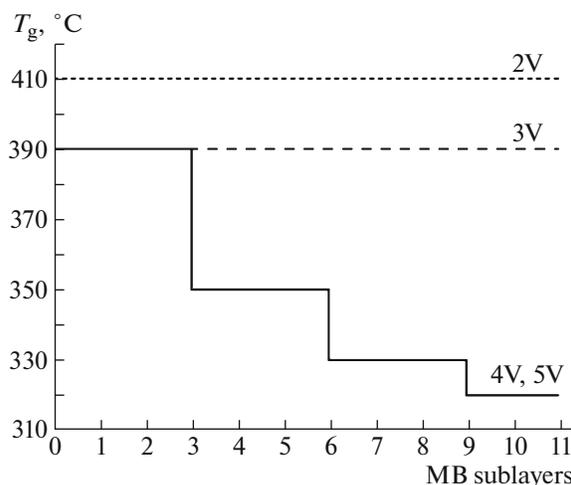


Fig. 2. Temperature modes of MB growth on the samples.

in turn, is generally limited by the requirements to the structural characteristics. Therefore, to obtain desired electrical properties for specific applications, one must use a limited range of technological conditions in each case and choose a substrate of certain type.

The surface morphology of the structures grown at standard growth temperatures on GaAs(100) and ($n11$) A ($n = 1-4$) substrates was investigated in detail in [25]. It was shown that the surface morphology depends strongly on the arsenic pressure (or the ratio γ of the As and Ga pressures), substrate type and orientation, and the doping level (which is set by the silicon-cell temperature).

The set of the samples under study provides variation in all the above factors. In addition, an MB and low-temperature growth mode are used, which should additionally affect the sample surface morphology.

Figures 3 and 4 present AFM and SEM images of the sample surfaces; the surface roughness rms values, determined by AFM measurements, are given in Table 2. These data indicate that the morphology of the sample surface and its roughness depend strongly on the growth temperature of the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layer, substrate orientation, and the doping level of the active layer.

Table 1. Technological conditions for growing the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layer

Sample	T_g , °C	Doping	P_{As4} , 10^{-5} Torr	γ
2V	450	absent	1.5	22
3V	450	Si	2.0	29
4V	200	absent	2.0	29
5V	200	Si	2.0	29

T_g is the growth temperature, P_{As4} is the arsenic-flow pressure, and γ is the flow ratio of the V- and III-group elements.

Table 2. Electrical parameters of the samples (electron mobility μ_e and electron concentration n) and the rms surface roughness R_q

Sample	$T_g, ^\circ\text{C}$	Active-layer dopant	$\mu_e, \text{cm}^2/(\text{Vs})$	$n \times 10^{16}, \text{cm}^{-3}$	R_q, nm
2V-0	450	absent	2250	4.2	28
2V-1	450	absent	497	0.8	65
3V-0	450	Si	3340	222.1	33
3V-1	450	Si	1360	245.7	55
4V-0	200	absent	383	18.4	12
4V-1	200	absent	109	30.9	16
5V-0	200	Si	1920	270.6	4.4
5V-1	200	Si	231	165.4	11

The surface morphology of the samples of series 2V and 3V significantly differs from that for the samples of series 4V and 5V (Figs. 3, 4). The surface is dotted with depressions in the form of orthorhombic pyramids 0.1–0.6 μm in size. At the same time, the samples on GaAs(111)A substrates have a strongly faceted surface. The occurrence of pyramidal defects is generally related to the presence of excess Ga atoms on the growing surface during epitaxial growth [26]. This situation is more likely for the samples of series 2V and 3V, because, with identical typical technological growth conditions of the MB, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ active layers of these samples were grown in the high-temperature mode. As follows from [27], pronounced square and rectangular elements are observed on the

surface of InGaAs layers grown at a temperature differing from optimal. In this case, the desorption of As and In atoms from the growing surface is enhanced because of the heating with simultaneous enhancement of the segregation of In atoms. These processes increase the surface roughness.

It was shown by the AFM analysis (Table 2) that the surfaces on which pyramidal defects dominate (samples of series 2V and 3V) are characterized by a higher roughness. The formation of three-dimensional pyramidal defects can also be due to the local elastic stress in the films. As follows from [28], the residual elastic stress in metamorphic structures depends on not only the MB compositional gradient but also on the MB dopant type (Be or Si). However, in contrast to [28], where the doping of the MB with Si atoms increased the surface roughness, Si atoms were used in this study to dope the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layer. At the high-temperature growth of the active layer (samples 2V and 3V), the doping with Si atoms increased the roughness R_q for samples on GaAs(100) substrates and reduced it for samples on GaAs(111)A substrates.

Let us consider the samples of series 4V and 5V. It can be seen in Figs. 3 and 4 that the sample surfaces are granular, with a grain size of 0.1–0.2 μm . The surface of sample 5V(100) has a transverse-stripe relief, characteristic of metamorphic heterostructures with the smallest roughness among the samples under investigation. It can be seen in Table 2 that the doping of the low-temperature $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ active layers grown on substrates of both types with Si atoms leads

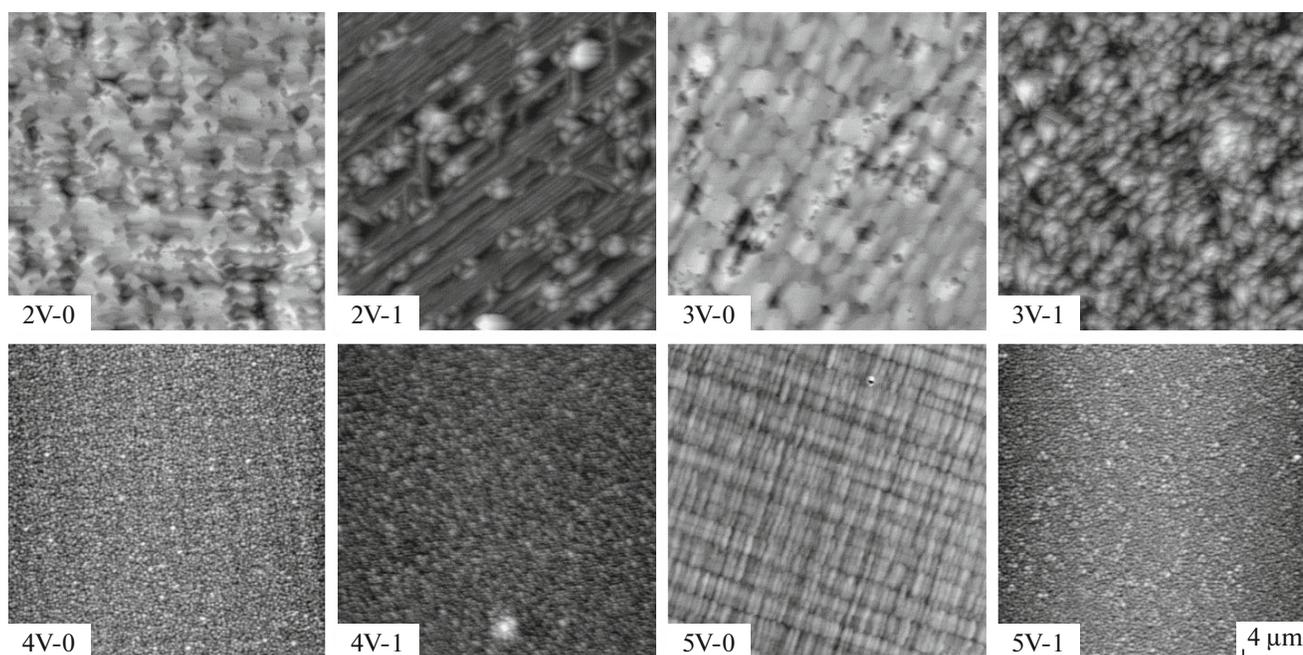


Fig. 3. AFM surface images of the samples; the scan area is $20 \times 20 \mu\text{m}$.

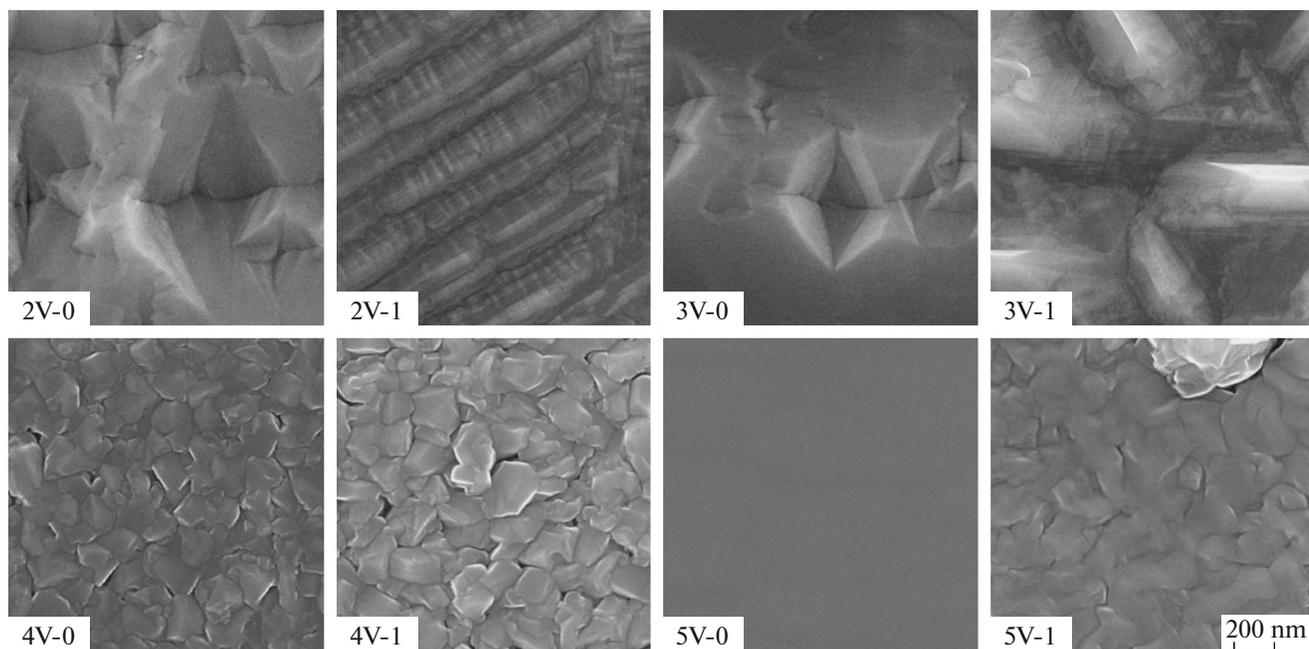


Fig. 4. SEM surface images of the samples; the scan area is $1.52 \times 1.52 \mu\text{m}$.

to a decrease in their surface roughness. A similar case was described in [25], where it was noted that the surface roughness of structures on GaAs(100) and GaAs(111)*A* substrates decreases at a certain level of doping with Si.

Specific Features of the Crystal Structure

Figures 5 and 6 present bright-field PREM images of transverse cuts of the samples under study. Let us consider the images of the MB of the samples on GaAs(100) substrates (Figs. 5a, 5c, 6a, 6c). The first 7–9 steps of the MB are clearly distinguishable, while the upper steps are less pronounced. Dislocations oriented parallel to the interfaces can be seen in the MB steps. The type and density of the dislocations in the MB are beyond the scope of this study. Dark stripes oriented perpendicular to the interfaces can be seen in the MB and in a part of the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layer in the sample shown in Fig. 5c. They are likely caused by the small-angle boundaries between the domains formed in the MB. The stripe contrast almost disappears at the substrate–MB interfaces, which is an evidence for this suggestion.

The PREM image of the MB of sample 2V-1 on GaAs(111)*A* substrates is given in Fig. 5b. The first three MB steps, which are located directly above the substrate, are distinguishable. The density of dislocations, which grow in perpendicular to the substrate surface, is low; however, some other features are pronounced: oblique stacking faults and microtwins. These defects are located in the planes oriented parallel to $(\bar{1}11)$ plane, making an angle of $\sim 70^\circ$ with the

(111) surface; their nature will be considered elsewhere. Contrast variations parallel to the (211) plane can also be seen in the images of these layers. The occurrence of these stripes can be explained by oblique stacking faults lying in the plane oriented parallel to $(\bar{1}\bar{1}1)$ plane, making some angle with the cut surface. The influence of twinning dislocations and the related stress may also occur. A faceted line in the form of a chain of triangular fragments, which have a horizontal size of 200–700 nm and a vertical size of 100–200 nm, can be seen at a distance of 200–400 nm from the substrate–MB interface. In the bright-field PREM image (Fig. 7), this line has a dark contrast; numerous dislocations go upwards from it (characteristic black-and-white wavy lines). The upper MB boundary (MB– $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$) is much less pronounced in these images; however, it can be seen in some images that this interface is also a broken line. Hence, one can suggest that, after reaching some critical thickness (~ 130 nm), the initial planar growth of the MB changes to three-dimensional growth with preferred formation of large pyramidal islands. The fact that the MB steps can be seen above the broken interface at some thickness can be explained by the superposition of three-dimensional growth regions and the regions where the planar growth is still continued. This situation was observed most clearly in the MB of samples 2V-1 and 3V-1 (Figs. 5b, 5d). Note that no such changes in the growth mode were observed in the PREM images recorded in the previous investigations of the LT-GaAs films grown on GaAs(111)*A* substrates [29]. Therefore, we can suggest that the change in the growth mode is due to the relaxation of elastic stress in

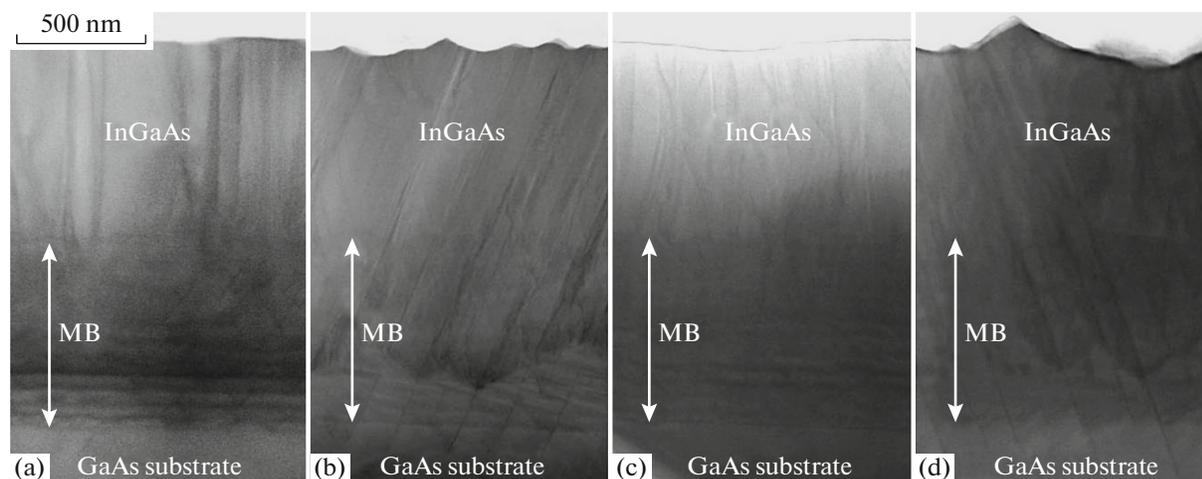


Fig. 5. Bright-field PREM images of the samples with a high-temperature active layer: (a) 2V-0, (b) 2V-1, (c) 3V-0, and (d) 3V-1.

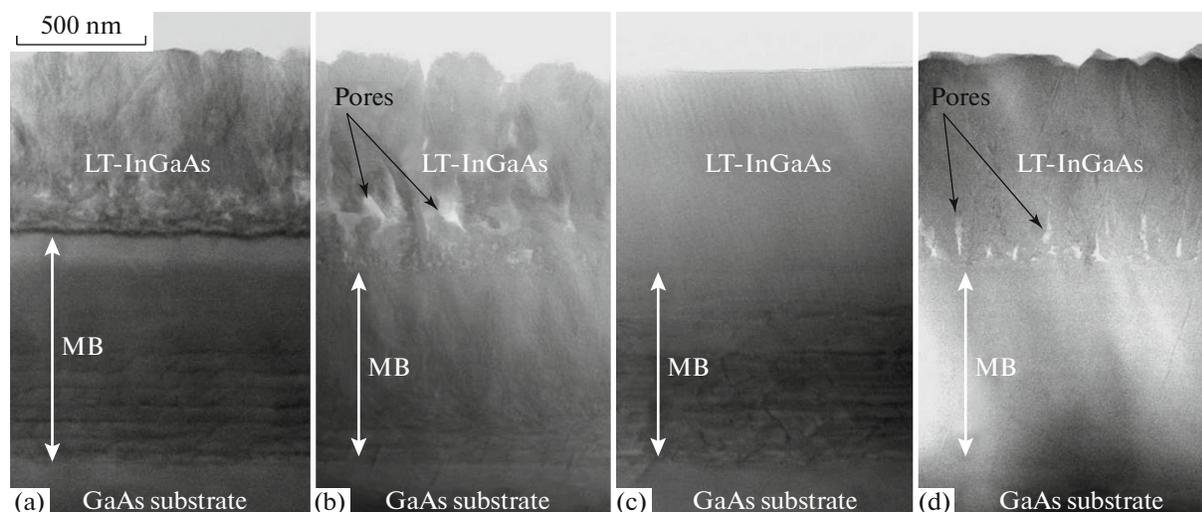


Fig. 6. Bright-field PREM images of the samples with a low-temperature active layer: (a) 4V-0, (b) 4V-1, (c) 5V-0, and (d) 5V-1.

the MB in specifically these two samples. This is also evidenced by the fact that numerous threading dislocations are formed directly after the broken interface.

A clear separation of the MB steps by thin bright stripes in the dark-field high-angle PREM images for all the samples indicates that the interfaces are enriched with indium due to the segregation of In atoms during the stop of the MB epitaxial growth, which is necessary to change the temperature of the In molecular source and stabilize the molecular flow before growing the next MB step. The growth interruption time between steps in the experiment was 2 min.

A detailed study showed that stacking faults threading through the film were observed in all the samples grown on GaAs(111) \bar{A} substrates; however, their concentration in samples 2V-1 and 3V-1 was much higher than that in samples 4V-1 and 5V-1. In addition, in all

the samples on the (111) \bar{A} substrates, microtwins are observed near the MB and at the top of the substrate (Fig. 8), and additional reflections, typical of twinning in fcc structures, are observed in the electron diffraction patterns (see inset).

High-temperature $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers (samples 2V and 3V) (Figs. 5a–5d) appear to be family homogeneous. In the samples on GaAs(100) substrates, they are threaded by vertical dislocations and small-angle boundaries beginning in the MB. The density of dislocations and small-angle boundaries in the active region of sample 3V-0 was estimated to be lower than that in sample 2V-0; this result is consistent with the much higher electron mobility in sample 3V-0 in comparison with sample 2V-0.

Low-temperature $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers of samples 4V-0, 4V-1, and 5V-1 (Figs. 6a, 6b, 6d) are divided into two different sublayers. The lower and upper sub-

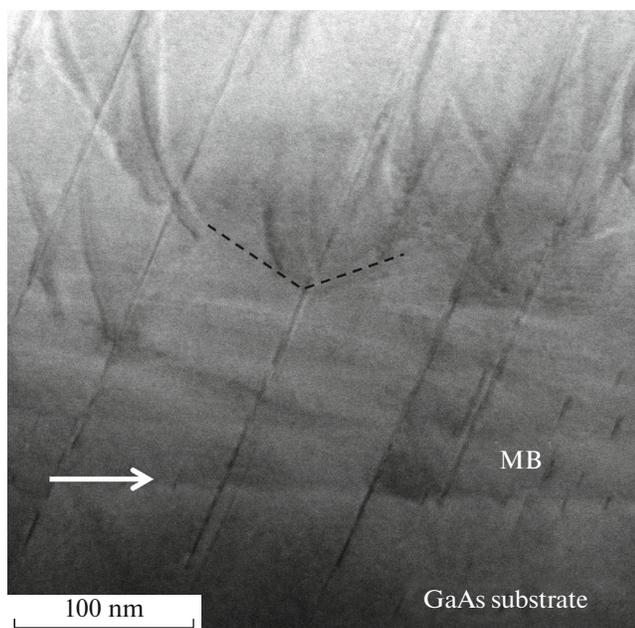


Fig. 7. Bright-field PREM image of the lower part of sample 2V-1; the arrow indicates the interface with the substrate, and the dotted line selects the region of triangular-fragment formation.

layers have thicknesses of 100–250 and 550–700 nm, respectively. An exception is sample 5V-0, where the LT-In_{0.5}Ga_{0.5}As layer appears to be homogeneous and defect-free. We should also note that the surface of sample 5V-0 has the least roughness among all the samples under study, and a regular transverse-stripe relief that is characteristic of metamorphic structures is formed on only this surface. The lower sublayer can arbitrarily be referred to as a region of domain formation (it consists of small domains and contains pores), while the upper sublayer can be called a region of formed domains (it consists of large domains, which were formed upon aggregation of small domains from the lower sublayer). An electron diffraction study shows that the misorientation of individual domains, both small and large, does not exceed 3°.

Note the better quality of the crystal structure of the active region of sample 5V-0 (Fig. 6c) in comparison with sample 4V-0 (Fig. 6a), which is also confirmed by a higher electron mobility in sample 5V-0 in comparison with sample 4V-0. Both samples were grown in the low-temperature mode, and the only difference is that the active region of sample 5V-0 is Si-doped. The improvement of the structural quality of this sample can be caused by two factors. First, doping with silicon, as was noted above, improves the surface morphology under certain conditions and, accordingly, increases the structural quality of the epitaxial layer. Second (this factor is likely decisive), the heated and open silicon molecular source additionally heats the film surface during epitaxial growth. In the exper-

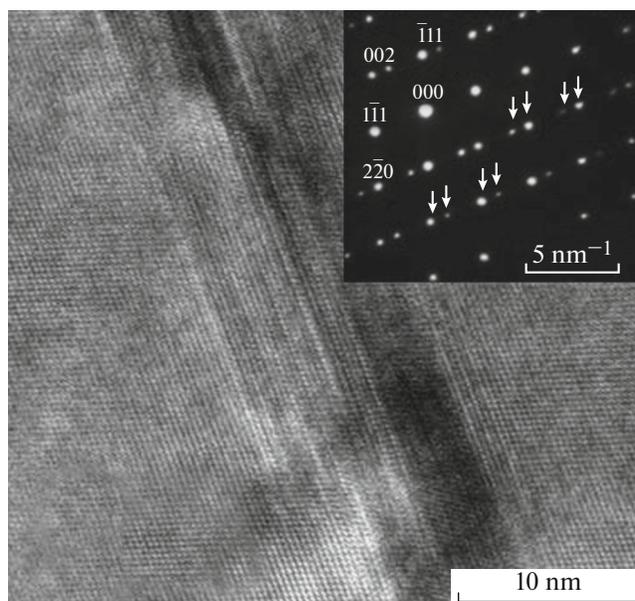


Fig. 8. Bright-field TEM image of a twin and an electron diffraction pattern of the region of sample 2V-1 (inset) containing a twin (the arrows in the electron diffraction pattern indicate doubled reflections).

iment, the silicon source temperature was 1120°C. Dopant sources in MBE systems are known to increase the true growth temperature (settled and measured by a thermocouple) by about 50°C [30]. Additional heating of the sample due to the strongly heated molecular sources depends, undoubtedly, on the design features of a specific system and, according to estimations, may be as high as 80°C. In view of the aforesaid, one can suggest that the true growth temperature of samples 5V-0 and 5V-1 was higher than found one by about 50–70°C (it was equal to ~250–270°C). Since the doping was homogeneous, annealing of the LT-In_{0.5}Ga_{0.5}As layer lasted during the entire growth process. This is the reason for the difference between the microstructures of the samples of series 4V and 5V.

There are pores in the lower LT-In_{0.5}Ga_{0.5}As sublayers of samples 4V-0, 4V-1, and 5V-1 (Figs. 6a, 6b, 6d). In samples 4V-0 and 4V-1, they have an irregular shape and sizes of 70–130 nm. In sample 5V-1, pores are elongated (height 70–130 nm, width 15–25 nm) and mainly oriented vertically. The energy-dispersive spectra of neighboring portions with a pore and without it basically coincided; however, the signal intensity from the pore was lower by an order of magnitude. As in [29], these data confirm that the aforementioned regions are pores, which are not enriched in any atoms. The presence of pores leads to a difference in the thicknesses of individual parts of the formed-domain region and a pronounced surface morphology.

CONCLUSIONS

Electrical characteristics, surface morphology, and specific features of the microstructure of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ epitaxial films grown by the MBE method on GaAs(100) and GaAs(111)*A* substrates using a step-graded metamorphic $\text{In}_x\text{Ga}_{1-x}\text{As}$ buffer were investigated. The $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ films were grown in the standard and low-temperature modes (450 and 200°C, respectively); they were either undoped or homogeneously doped with Si.

It was shown that, under the technological conditions where the Si-doped GaAs layer on a GaAs(111)*A* substrate acquires *p*-type conductivity, the Si-doped LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layer on a GaAs(111)*A* substrate retains electronic conductivity.

It was shown that, at a growth temperature of 450°C, the rms roughness of the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ surface is higher by a factor of 2.3–7.5 than that observed at a growth temperature of 200°C and that the use of a (111)*A* substrate increases the rms roughness by a factor of 1.3–2.5 as compared with the (100) orientation. Doping with silicon under the low-temperature growth conditions leads mainly to a decrease in the rms roughness of the films grown on both GaAs(100) and GaAs(111)*A* substrates (it changes by a factor of 0.4–0.8).

The LT- $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ layers were shown to consist of two sublayers. Small domains and pores 10–80 nm in size are formed in the lower sublayer (100–250 nm thick). The upper sublayer (550–700 nm thick) is a region of formed domains and consists mainly of large vertical domains ~200–250 nm in size. An electron diffraction study showed that the misorientation of individual domains does not exceed 3°.

ACKNOWLEDGMENTS

We are grateful to I.S. Vasil'evskii and R.R. Galiev for their help in AFM and SEM measurements.

This study was supported by the Russian Foundation for Basic Research, project no. 16-29-03294 of_i_m.

REFERENCES

1. I. S. Gregory, C. Baker, W. R. Tribe, et al., *Appl. Phys. Lett.* **83** (20), 4199 (2003).
2. C. Baker, I. S. Gregory, E. R. Tribe, et al., *Appl. Phys. Lett.* **85** (21), 4965 (2004).
3. H. Eusebe, J.-F. Roux, J.-L. Coutaz, et al., *J. Appl. Phys.* **98**, 033711 (2005).
4. A. Krotkus, *J. Phys. D: Appl. Phys.* **43**, 273001 (2010).
5. N. Kim, S.-P. Han, H. Ko, et al., *Opt. Express* **19** (16), 15397 (2011).
6. A. Krotkus, K. Bertulis, L. Dapkus, et al., *Appl. Phys. Lett.* **75**, 3336 (1999).
7. A. Takazato, M. Kamakura, T. Matsui, et al., *Appl. Phys. Lett.* **91**, 011102 (2007).
8. M. D. Vilisova, I. V. Ivonin, L. G. Lavrent'eva, et al., *Fiz. Tekh. Poluprovodn.* **33** (8), 900 (1999).
9. A. Takazato, M. Kamakura, T. Matsui, et al., *Appl. Phys. Lett.* **90**, 101119 (2007).
10. B. Sartorius, H. Roehke, H. Kunzel, et al., *Opt. Express* **16** (13), 9565 (2008).
11. S. Bollaert, Y. Cordier, M. Zaknoute, et al., *Solid-State Electronics*. **44** (6), 1021 (2000).
12. Y. Cordier, P. Lorenzini, J.-M. Chauveau, et al., *J. Cryst. Growth* **251**, 822 (2003).
13. K. Elgaid, H. McLelland, and M. Holland, *IEEE Electron Device Lett.* **26** (11), 784 (2005).
14. J. J. Komiak, P. M. Smith, K. H. G. Duh, et al., *Proc. IEEE Compound Semiconductor Integrated Circuit Symposium, Monterey, California, USA, October 13–16, 2013*, p. 133.
15. Y. Song, S. Wang, X. Cao, et al., *J. Cryst. Growth* **323**, 21 (2011).
16. I. Tangring, S. M. Wang, M. Sadeghi, et al., *J. Cryst. Growth* **281**, 220 (2005).
17. V. Bellani, C. Bocchi, T. Ciabattini, et al., *Eur. Phys. J. B* **56**, 217 (2007).
18. Y. Song, S. Wang, I. Tangring, et al., *J. Appl. Phys.* **106**, 123531 (2009).
19. G. B. Galiev, S. S. Pushkarev, I. S. Vasil'evskii, et al., *Semiconductors* **47** (7), 997 (2013).
20. G. B. Galiev, S. S. Pushkarev, E. A. Klimov, et al., *Crystallogr. Rep.* **59** (2), 258 (2014).
21. F. Romanato, E. Napolitani, A. Carnera, et al., *J. Appl. Phys.* **86** (9), 4748 (1999).
22. G. Galiev, V. Kaminskii, D. Milivzorov, et al., *Semicond. Sci. Technol.* **17** (2), 120 (2002).
23. G. B. Galiev, V. G. Mokerov, Yu. V. Slepnev, et al., *Zh. Tekh. Fiz.* **69** (7), 68 (1999).
24. G. B. Galiev, I. S. Vasil'evskii, E. A. Klimov, et al., *J. Mater. Res.* **30** (20), 3020 (2015).
25. T. Ohachi, J. M. Feng, K. Asai, et al., *Microelectronics J.* **30**, 471 (1999).
26. K. Sato, M. R. Fany, and B. A. Joyce, *Jpn. J. Appl. Phys.* **33**, L905 (1994).
27. F. Peiro, A. Cornet, J. R. Morante, et al., *J. Appl. Phys.* **83** (12), 7537 (1998).
28. I. Tangring, Y. X. Song, Z. H. Lai, et al., *J. Cryst. Growth* **311** (7), 1684 (2009).
29. G. B. Galiev, E. A. Klimov, A. L. Vasil'ev, et al., *Crystallogr. Rep.* **62** (1), 82 (2017).
30. M. Missous, *Microelectron. J.* **27**, 393 (1996).

Translated by A. Sin'kov